



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,674	07/03/2001	Patrick H. Mawet	MEIP117200	2329

26389 7590 05/07/2003

CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC  
1420 FIFTH AVENUE  
SUITE 2800  
SEATTLE, WA 98101-2347

EXAMINER

TSAI, CAROL S W

ART UNIT

PAPER NUMBER

2857

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/898,674

Applicant(s)

MAWET, PATRICK H.

Examiner

Carol S Tsai

Art Unit

2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19 and 36 is/are allowed.
- 6) ☒ Claim(s) 1-8, 14, 15, 20-26, 31 and 32 is/are rejected.
- 7) ☒ Claim(s) 9-13, 16-18, 27-30 and 33-35 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 and 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

---

**DETAILED ACTION**

***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

Reference numbers "160 F" and "160G" shown on Fig. 2.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 4,020,487 to Winter.

Winter discloses a signal processing system suitable for processing transducer signals in a low power measuring instrument (see col. 5, lines 5-12), the signal processing system comprising; a reference signal generator (ramp generator 20 shown on Fig. 1) for generating an ADC ramp signal (see col. 3, lines 41-43); two or more differential signal channels, each differential signal channel comprising: a first comparator (comparator 16 shown on Fig. 1)

---

comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and a second comparator (comparator 18 shown on Fig. 1) comprising a first input, a second input, and an output, the first input of the second comparator receiving the second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the signals at the first and second inputs (see Fig. 1 and col. 3, lines 37-58); and one or more digital differential value determining circuits (logic circuit 24 shown on Fig. 1) for receiving the first-comparator output signal and the second-comparator output signal of at least one of the differential signal channels and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel; wherein the signal processing system is operable from a low voltage power supply to process the signals of the at least two differential signal channels in parallel and determine the corresponding digital values in parallel (see Fig. 1 and col. 7, lines 7-44).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-5 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of U. S. Patent No. 5,459,427 to Chambers et al.

As noted above, with respect to claims 2-5, Winter discloses the claimed invention, except for a signal processing system being operable from a low voltage power supply providing a voltage less than 3.5 volts.

Chambers et al. teach the signal processing system being operable from a low voltage power supply providing a voltage less than 3.5 volts (see col. 3, line 60 to col. 4, line 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include the signal processing system being operable from a low voltage power supply providing a voltage less than 3.5 volts, as taught by Chambers et al., in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see Chambers et al. col. 4, lines 2-4).

As to claims 20-24, Winter also discloses a signal processing method suitable for processing transducer signals (see col. 5, lines 5-12) in a low power measuring instrument, the signal processing method comprising; generating an ADC ramp signal (see col. 3, lines 41-43); for each of at least two differential signal channels; receiving the first signal of a pair of differential signals at a first input of a first comparator of the differential signal channel and receiving the ramp signal at a second input of the first comparator of the differential signal channel; outputting a first-comparator output signal based on the signals at the first and second inputs of the first comparator; and receiving the second signal of a pair of differential signals at a first input of a second comparator of the differential signal channel and receiving the ramp

---

signal at a second input of the second comparator of the differential signal channel; outputting a second-comparator output signal based on the signals at the first and second inputs of the second comparator (see Fig. 1 and col. 3, lines 37-58); and determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel based on the first-comparator output signal and the second-comparator output signal of that differential signal channel; wherein the generating, receiving, outputting and determining steps are performed to determine the digital values corresponding to each differential channel in parallel (see Fig. 1 and col. 7, lines 7-44).

Winter does not disclose generating, receiving, outputting and determining steps being performed using voltage signals which do not exceed 3.5 volts.

Chambers et al. teach generating, receiving, outputting and determining steps being performed using voltage signals which do not exceed 3.5 volts (see col. 3, line 60 to col. 4, line 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include generating, receiving, outputting and determining steps being performed using voltage signals which do not exceed 3.5 volts, as taught by Chambers et al., in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see Chambers et al. col. 4, lines 2-4).

---

6. Claims 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of Chambers et al. as applied to claims 1, 4, 5, 20, 22, and 24 above, and further in view of U. S. Patent No. 4,514,476 to Fitzgerald.

As noted above, with respect to claims 6 and 25, Winter in combination with Chambers et al. teach all the features of the claimed invention, but do not disclose a 1.5 volts button type battery.

Fitzgerald teaches a 1.5 volts button type battery (see col. 5, lines 52-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al.'s system to include a 1.5 volts button type battery, as taught by Fitzgerald, in order to provide sufficient electrical energy to power an measuring device.

7. Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of Chambers et al. as applied to claims 1, 4, 20, 22, and 24 above, and further in view of U.S. Patent No. 6,011,389 to Masreliez et al.

As noted above, with respect to claims 7 and 26, Winter in combination with Chambers et al. teach all the features of the claimed invention, but do not disclose portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation.

Masreliez et al. teach the portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation (see col. 22, lines 13-21).

---

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al.'s system to include the portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation, as taught by Masreliez et al., in order that the driving circuit can be able to provide a low duty cycle, and provide a strong output signal from the receiver winding, while still using a very small average current and a rapid sampling rate (see Masreliez et al. col. 22, lines 23-27).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of U. S. Patent No. 6,508,122 to McCall et al.

As noted above, Winter discloses the claimed invention, except for a circuit being fabricated on a single silicon substrate in an integrated circuit.

McCall et al. teach the circuit being fabricated on a single silicon substrate in an integrated circuit (see col. 2, lines 8-15 and col. 4, lines 25-31).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include the circuit being fabricated on a single silicon substrate in an integrated circuit, as taught by McCall et al., in order to obtain highly accurate, sensitive, stable angular rate measurements under dynamic environments (see McCall et al. col. 2, lines 12-14).

9. Claims 14 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of U. S. Patent No. 3,665,305 to Petrohilos.



---

As noted above, with respect to claims 14 and 31, Winter discloses the claimed invention, except for an ADC ramp signal generated by the reference signal generator comprising a linear single ramp reference signal.

Petrohilos teaches the ADC ramp signal generated by the reference signal generator comprising a linear single ramp reference signal (see Abstract, lines 1-6; col. 1, lines 34-41; and col. 3, lines 55-71).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include the ADC ramp signal generated by the reference signal generator comprising a linear single ramp reference signal, as taught by Petrohilos, in order that as long as the ramp output signal varies at a linear rate with respect to time, the actual rate of change or slope of the ramp output signal will not adversely affect the digital output from the device (see Petrohilos, col. 1, lines 39-42).

10. Claims 15 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of U. S. Patent No. 6,011,389 to Masreliez et al.

As noted above, with respect to claims 15 and 32, Winter disclose the claimed invention, except for a low power measuring instrument operable to determine a measurement based on the digital values.

Masreliez et al. teach the low power measuring instrument operable to determine a measurement based on the digital values (see col. 11, lines 1-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include the low power measuring instrument

---

operable to determine a measurement based on the digital values, as taught by Masreliez et al., in order that little power can be consumed to allow the transducer to be readily incorporated into hand-held, batter-powered measurement tools (see Masreliez et al. Abstract, lines 16-19).

*Allowable Subject Matter*

11. Claims 9-13, 16-18, 27-30, and 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 19 and 36 are allowed.

13. The following is a statement of reasons for the indication of allowable subject matter:

U. S. Patent No. 4,020,487 to Winter is the reference closest to the claimed invention.

Winter discloses a signal processing system suitable for processing transducer signals in a low power measuring instrument, the signal processing system comprising; a reference signal generator for generating an ADC ramp signal; one or more differential signal channels, each differential signal channel comprising: a first comparator comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and a second comparator comprising a first input, a second input, and an output, the first input of the second comparator receiving the second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the

---

signals at the first and second inputs; and one or more digital differential value determining circuits for receiving the first-comparator output signal and the second-comparator output signal of at least one differential signal channel and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel. However, Winter does not teach the one or more digital differential value determining circuits comprising at least one clock circuit configured such that for at least one comparator included in the clock circuit a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal input to the comparator being both controlled based on a common signal, such that variations in a voltage supplied to the clock during normal operation does not substantially affect the clock period; and including all of the other limitations in the respective independent claims.

### *Conclusion*

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yang et al. disclose a circuit including an analog-to-digital (A/D) converter for multiplexing between a numbers of analog input signals and converting the selected analog input signals to a digital code representation.

Nakaigawa discloses an A/D converter including a resistor ladder for generating a plurality of reference potentials, a comparing section for comparing each of the reference

---

potentials against an input analog signal to output a thermometric code, and a dynamic encoder composed of a combinational circuit to encode the thermometric code to a binary code by responding a clock signal.

Andoh et al. disclose an analog-to-digital (A/D) converter capable of receiving a differential input for improved noise rejection and having two static resistive ladders for reducing power consumption.

Vitunic discloses a circuit for powering a three-phase AC induction motor.

Kuwano et al. disclose an analog/digital converter providing a high conversion speed and resolution while greatly reducing the number of circuit elements.

Gulczynski discloses the true flash analog-to-digital converter having an extremely high speed and resolution.

Hotta et al. disclose a cyclic averaging analog to digital converter, reference voltages having a plurality of levels, each of which is inputted to one of a plurality of comparators in a flash type analog to digital converter, being shifted cyclically by a small voltage, and the outputs of the flash type analog to digital converter being added for every shift cycle in order to obtain an output digital signal.

### ***Contact Information***

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. Tsai whose telephone number is (703) 305-0851. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can

Art Unit: 2857

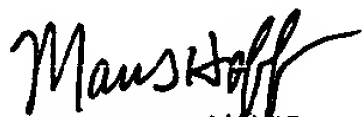
---

be reached on (703) 308-1677. The fax number for TC 2800 is (703) 308-7382. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (703) 308-1782.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 308-7382. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. Tsai

04/23/03

  
MARC S. HOFF  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800